CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) An integrated circuit die, comprising:

a device wafer portion having a face side surface, the device wafer portion comprising a semiconductor wafer portion and an interconnect portion, the interconnect portion having a surface that is the face side surface of the device wafer, the semiconductor wafer portion comprising a source region of a first conductivity type, a drain region of the first conductivity type and a channel structure of a second conductivity type opposite the first conductivity type, wherein the source region, the drain region and the channel structure are parts of a single layer of a semiconductor material and together form an island of the semiconductor material; and

a supporting structure portion that is bonded to the face side surface of the device wafer portion;

wherein the island extends outward from a back side surface of the interconnect portion opposite the face side surface of the device wafer portion.

2. (Original) The integrated circuit die of claim 1, wherein the island of semiconductor material has a substantially planar bottom surface, the source region having a bottom surface that makes up a part of the substantially planar bottom surface of the island, the drain region having a bottom surface that makes up another part of the substantially planar bottom surface of the island, wherein the planar bottom surfaces of the source and drain regions are not in contact with any semiconductor material of the semiconductor wafer portion of the device wafer.

3. (Original) The integrated circuit die of claim 1, wherein the channel structure has a key-shape.

4. (Original) The integrated circuit die of claim 1, wherein the supporting structure is a semiconductor wafer that is wafer-bonded to the face side surface of the device wafer portion.

5. (Original) The integrated circuit die of claim 1, wherein the semiconductor wafer portion of the device wafer comprises a plurality of islands, each of the islands comprising a source region, a drain region, and a channel structure.

6. (Original) The integrated circuit die of claim 1, wherein the source region has substantially no junction capacitance other than a junction capacitance between the source region and a channel structure.

7. (Original) The integrated circuit die of claim 1, wherein the island consists essentially of the source region, the drain region and the channel structure.

8. (Currently Amended) A transistor structure, comprising:

a device wafer having a substantially planar face side, the device wafer comprising:

a gate;

a source region;

a drain region; and

means for providing a conductive channel between the source region and the drain region such that substantially the only junction capacitance on the source region is a junction capacitance due to an interface between the source region and the means; and

a supporting structure that is wafer-bonded to the face side of the device wafer; the device wafer having a back side opposite the face side, wherein at least one

surface of at least one of the source region and the drain region substantially normal to the back side is exposed.

9. (Original) A transistor structure of claim 8, wherein the device wafer comprises an island of semiconductor material, and wherein the island of semiconductor material consists essentially of the source region, the drain region, and the means.

10. (Original) The transistor structure of claim 8, wherein the means is a key-shaped feature of a semiconductor material, and wherein the source region is in contact with no semiconductor material other than the means.